IN THE CLAIMS:

Please amend claim 6 as follows.

1. (Original) A method for synchronization adaptation of asynchronous digital data streams comprising the steps of

providing a first digital data stream (PCM_IN) at a first sample rate (CLK_1);

inputting said first digital data stream (PCM_IN) to a sample rate conversion means (SRC);

supplying data output from said sample rate conversion means (SRC) to a processing element (BUFFER);

storing said supplied data into said processing element (BUFFER); and

outputting said data stored in said processing element as a second digital data stream (PCM_OUT) at a second sample rate (CLK_2), with said first and said second sample rates (CLK_1, CLK-2) being different from each other;

characterized by the further steps of

detecting a state (BUFFER_STATUS) of said processing element (BUFFER); and

controlling said sample rate conversion means (SRC) dependent on the detected state of said processing element.

2. (Original) A method for synchronization adaptation of asynchronous digital data streams according to claim 1,

characterized in that

said state (BUFFER_STATUS) of said processing element (BUUFER) represents the amount of data currently stored in said processing element.

3. (Original) A method for synchronization adaptation of asynchronous digital data streams according to claim 2,

characterized in that

said detection step comprises the steps of

comparing a current amount of data stored in said processing element with a lower limit (LL) and an upper limit (UL) of respective admissible data amounts stored in said processing element, and

setting said state (BUFFER_STATUS) of said process element

to a first value (FULL) in case the detected actual amount of stored data exceeds the upper limit (UL),

to a second value (EMPTY) in case the detected actual amount of stored data is below the lower limit (LL), and

to a third value (OK) in case the detected actual amount of stored data is found to be between the lower limit (LL) and the upper limit (UL).

4. (Original) A method for synchronization adaptation of asynchronous digital data streams according to claim 3,

characterized in that

said controlling step controls said sample rate conversion means to be enabled if said detected state (BUFFER_STATUS) has said first (FULL) or said second (EMPTY) value, and to be disabled if said detected state has said third value (OK).

5. (Previously Amended) A method for synchronization adaptation of asynchronous digital data streams according to claim 3,

characterized in that

said controlling step comprises the steps of

reducing the number of data samples contained in the data output by said sample rate conversion means (SRC) and supplied to said processing means if said state has said first value (FULL),

increasing the number of data samples contained in the data output by said sample rate conversion means (SRC) and supplied to said processing means if said state has said second value (EMPTY), and

leaving the number of data samples contained in the data output by said sample rate conversion means (SRC) and supplied to said processing means unchanged if said state has said third value (OK).

6. (Currently Amended) A method for synchronization adaptation of asynchronous digital data streams according to claim 1,

characterized in that

reducing and/or increasing a ~~the~~ number of data samples contained in the data output by said sample rate conversion means (SRC) and supplied to said processing means is randomized in time within the data stream, such that a ~~the~~ position within a ~~the~~ group where a sample is to be removed and/or to be added is randomly selected.

7. (Original) A device for synchronization adaptation of asynchronous digital data stream comprising

a sample rate conversion means (SRC) to which is input a first digital data stream (PCM_IN) at a first sample rate (CLK_1);

a processing element (BUFFER) for storing data output from said sample rate conversion means (SRC), and for outputting said data stored in said processing element as a second digital data stream (PCM_OUT) at a second sample rate (CLK_2), with said first and said second sample rates (CLK_1, CLK_2) being different from each other;

characterized by

a detection means for detecting a state (BUFFER_STATUS) of said processing element (BUFFER); and

a control means for controlling said sample rate conversion means (SRC) dependent on the detected state of said processing element.